IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
FRANCIS ET AL.)
)
Serial No. **Not Yet Assigned**)
)
Filing Date: **Herewith**)
)
For: **DEVICE AND METHOD FOR SELECTIVELY POWERING DOWN INTEGRATED CIRCUIT BLOCKS WITHIN A SYSTEM ON CHIP**)

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

EXPRESS MAIL NO: EL747059590US

DATE OF DEPOSIT: November 5, 2001

NAME: Jennifer Ferguson

SIGNATURE: Jennifer Ferguson

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for proposed drawing modifications as indicated in red ink to label FIGS. 1-3 as prior art. FIGS. 2, 3, 4 and 9 are being modified to remove extraneous markings therefrom as indicated in red ink. FIG. 6 is being modified to correct word spacings and include a box as indicated in red ink around the flow diagram. FIGS. 7 and 8 are also being modified as indicated in red ink to add lines connecting to the reference numerals.

In the Specification:

Please replace the paragraph beginning at page 5, lines 26-28, with the following rewritten paragraph:

-- One aspect of the invention is directed to a system-on-chip (SOC) comprising a plurality of circuit blocks, each responsive to a respective local clock signal. At least one system clock is connected to the circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals.

A power control manager is connected to the circuit blocks for selectively providing a shutdown signal thereto. Each circuit block comprises a local power control circuit for selectively maintaining the system clock signal as the local clock signal even after receiving the shutdown signal if the circuit block is in an active state when the shutdown signal is received. --

Please replace the paragraph beginning at page 5, lines 29-32, with the following rewritten paragraph:

-- Another aspect of the invention is directed to a method for powering down circuit blocks within a system-on-chip (SOC) comprising a plurality of circuit blocks. The method comprises providing a system clock signal to the circuit blocks for functioning as a respective local clock signal, selectively providing a shutdown signal to the circuit blocks, and selectively maintaining the system clock signal as the respective local clock signal block even after receiving the shutdown signal if the circuit block is in an active state when the shutdown signal is received. --

In the Claims:

Please cancel Claims 1 to 11.

Please add new Claims 12 to 37.

12. A system-on-chip (SOC) comprising:

a plurality of circuit blocks, each responsive to a respective local clock signal;

at least one system clock connected to said circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals;

a power control manager connected to said circuit blocks for selectively providing a shutdown signal thereto; and

each circuit block comprising a local power control circuit for selectively maintaining the system clock signal as the local clock signal even after receiving the shutdown signal if the circuit block is in an active state when the shutdown signal is received.

13. An SOC according to Claim 12, wherein each local power control circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the respective local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state.

14. An SOC according to Claim 12, wherein said power control manager is connected to each local power control circuit through a respective clock enable line for providing the shutdown signal thereto.

15. An SOC according to Claim 14, wherein each circuit block further comprises a block logic circuit having a

status line connected to said local power control circuit for providing a status signal thereto indicating whether said circuit block is in the active or idle state.

16. An SOC according to Claim 15, wherein each local power control circuit comprises a logic circuit having a first input connected to a respective clock enable line, a second input connected to a respective status line, a third input connected to said at least one system clock, and an output for providing the local clock signal based upon logic states of the shutdown signal, the status signal and the system clock signal.

17. An SOC according to Claim 14, wherein said power control manager comprises at least one register connected to the respective clock enable lines for storing data indicating logic states of the shutdown signals.

18. An SOC according to Claim 17, further comprising a central processing unit connected to said power control manager for determining whether each circuit block is in the active or idle state by querying said at least one register.

19. An SOC according to Claim 12, wherein said at least one system clock comprises a plurality of system clocks, each system clock for providing the system clock signal to selected circuit blocks.

20. A system-on-chip (SOC) comprising:
a plurality of circuit blocks;
a system clock connected to said circuit blocks for

providing a system clock signal thereto; and

a power control manager connected to said circuit blocks for selectively providing a shutdown signal thereto;

each circuit block comprising

a block logic circuit providing a status signal indicating whether said circuit block is in an active or idle state, and

a local power control circuit for selectively maintaining the system clock signal as a local clock signal even after receiving the shutdown signal if the status signal indicates said circuit block is in the active state when the shutdown signal is received.

21. An SOC according to Claim 20, wherein each local power control circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state.

22. An SOC according to Claim 20, wherein said power control manager is connected to each local power control circuit through a respective clock enable line for providing the shutdown signal thereto.

23. An SOC according to Claim 22, wherein each local power control circuit comprises a logic circuit having a first input connected to a respective clock enable line, a second input connected to a respective status line, a third input connected to said system clock, and an output for providing

the local clock signal based upon logic states of the shutdown signal, the status signal and the system clock signal.

24. An SOC according to Claim 22, wherein said power control manager comprises at least one register connected to the respective clock enable lines for storing data indicating logic states of the shutdown signals.

25. An SOC according to Claim 24, further comprising a central processing unit connected to said power control manager for determining whether each circuit block is in the active or idle state by querying said at least one register.

26. A system-on-chip (SOC) comprising:

a plurality of circuit blocks;

a system clock connected to said circuit blocks for providing a system clock signal thereto;

a power control manager connected to said circuit blocks through a respective clock enable line for selectively providing a shutdown signal thereto, said power control manager comprising at least one register connected to the clock enable lines for storing data indicating logic states of the shutdown signals;

a central processing unit connected to said power control manager for determining whether each circuit block is in an active or idle state by querying said at least one register; and

each circuit block comprising a local power control circuit for selectively maintaining the system clock signal as a local clock signal even after receiving the shutdown signal if the circuit block is in the active state when the shutdown

signal is received.

27. An SOC according to Claim 26, wherein each local power control circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the local clock signal if said corresponding circuit block receiving the shutdown signal is in the idle state.

28. An SOC according to Claim 26, wherein said power control manager is connected to each local power control circuit through the respective clock enable line for providing the shutdown signal thereto.

29. An SOC according to Claim 26, wherein each circuit block further comprises a block logic circuit having a status line connected to said local power control circuit for providing a status signal thereto indicating whether said circuit block is in the active or idle state.

30. An SOC according to Claim 29, wherein each local power control circuit comprises a logic circuit having a first input connected to a respective clock enable line, a second input connected to a respective status line, a third input connected to said system clock, and an output for providing the local clock signal based upon logic states of the shutdown signal, the status signal and the system clock signal.

31. A method for powering down circuit blocks within a system-on-chip (SOC) comprising a plurality of circuit blocks, the method comprising:

providing a system clock signal to the circuit blocks for functioning as a respective local clock signal;

selectively providing a shutdown signal to the circuit blocks; and

selectively maintaining the system clock signal as the respective local clock signal block even after receiving the shutdown signal if the circuit block is in an active state when the shutdown signal is received.

32. A method according to Claim 31, further comprising preventing the system clock signal from functioning as the respective local clock signal if the corresponding circuit block receiving the shutdown signal is in an idle state.

33. A method according to Claim 31, wherein the SOC comprises a power control manager for providing the shutdown signals, and wherein each circuit block comprises a local power control circuit connected to the power control manager through a respective clock enable line for receiving the shutdown signal therefrom.

34. A method according to Claim 33, wherein each circuit block further comprises a block logic circuit having a status line connected to the local power control circuit for providing a status signal thereto indicating whether the circuit block is in the active or idle state.

35. A method according to Claim 34, wherein each local power control circuit comprises a logic circuit having a first input connected to a respective clock enable line, a

second input connected to a respective status line, a third input connected to a system clock, and an output for providing the respective local clock signal based upon logic states of the shutdown signal, the status signal and the system clock signal.

36. A method according to Claim 33, wherein the power control manager comprises at least one register connected to the respective clock enable lines for storing data indicating logic states of the shutdown signals.

37. A method according to Claim 36, further comprising querying the at least one register for determining whether each circuit block is in the active or idle state.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below. Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached paper is captioned "Version

In re Patent Application of:
FRANCIS ET AL.
Serial No. **Not yet assigned**
Filing Date: **Herewith**
______________________________/

With Markings to Show Changes Made."

Respectfully submitted,

MICHAEL W. TAYLOR
Reg. No. 43,182
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330
407-841-2343 fax
Attorneys for Applicants

In re Patent Application of:
FRANCIS ET AL.
Serial No. **Not yet assigned**
Filing Date: **Herewith**
_____/

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at page 5, line 26-28 has been amended as follows:

[Based on this idea, this invention provides a selective power down circuit as previously indicated and defined in the characterizing portion of Claim 1.] One aspect of the invention is directed to a system-on-chip (SOC) comprising a plurality of circuit blocks, each responsive to a respective local clock signal. At least one system clock is connected to the circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals.

A power control manager is connected to the circuit blocks for selectively providing a shutdown signal thereto. Each circuit block comprises a local power control circuit for selectively maintaining the system clock signal as the local clock signal even after receiving the shutdown signal if the circuit block is in an active state when the shutdown signal is received.

Paragraph beginning at page 5, line 29-32 has been amended as follows:

[Additionally, this invention provides a method for powering down individual circuit blocks within a system-on-chip as previously indicated and defined in the characterizing portion of Claim 7.] Another aspect of the invention is directed to a method for powering down circuit blocks within a system-on-chip (SOC) comprising a plurality of circuit blocks.

The method comprises providing a system clock signal to the circuit blocks for functioning as a respective local clock signal, selectively providing a shutdown signal to the circuit blocks, and selectively maintaining the system clock signal as the respective local clock signal block even after receiving the shutdown signal if the circuit block is in an active state when the shutdown signal is received.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
FRANCIS ET AL.

Serial No. **Not Yet Assigned**

Filing Date: **Herewith**

For: **DEVICE AND METHOD FOR SELECTIVELY POWERING DOWN INTEGRATED CIRCUIT BLOCKS WITHIN A SYSTEM ON CHIP**

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

EXPRESS MAIL NO: EL747059590US

DATE OF DEPOSIT: November 5, 2001

NAME: Jennifer Ferguson

SIGNATURE: Jennifer Ferguson

SUBMISSION OF PROPOSED MODIFICATIONS TO DRAWINGS

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Submitted herewith is a request for proposed drawing modifications as indicated in red ink to label FIGS. 1-3 as prior art. FIGS. 2, 3, 4 and 9 are being modified to remove extraneous markings therefrom as indicated in red ink. FIG. 6 is being modified to correct word spacings and include a box as indicated in red ink around the flow diagram. FIGS. 7 and 8 are also being modified as indicated in red ink to add lines connecting to the reference numerals.

Respectfully submitted,

Michael W. Taylor

MICHAEL W. TAYLOR
Reg. No. 43,182
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Ave., Suite 1401
P. O. Box 3791
Orlando, Florida 32802
(407) 841-2330
Attorney for Applicants

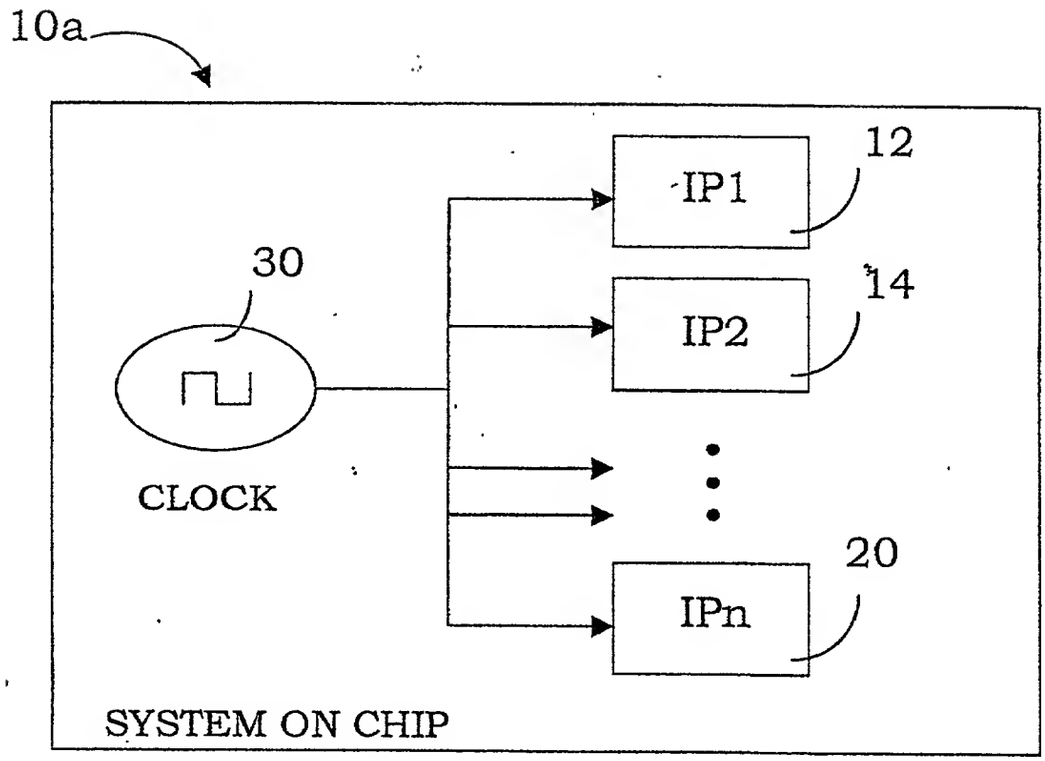

FIG. 1
(Prior Art)

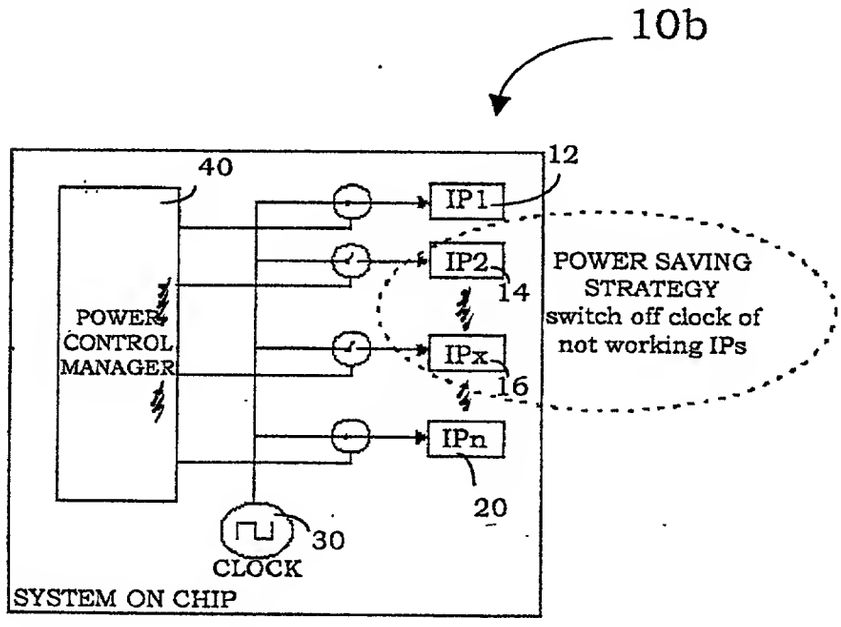

FIG. 2
(Prior Art)

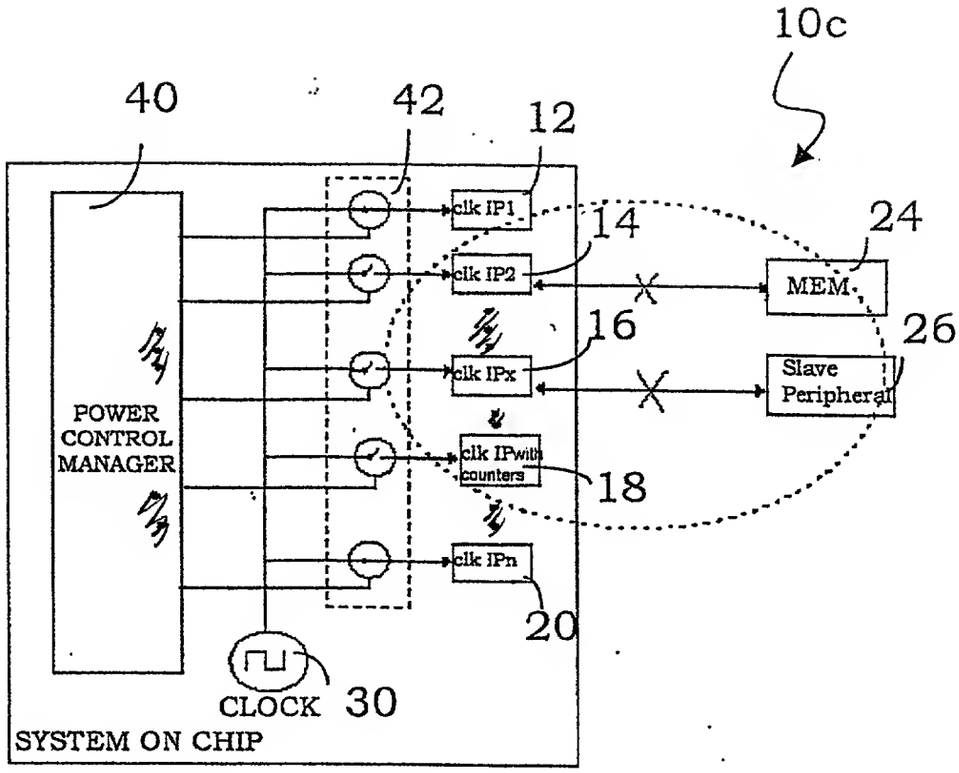

FIG. 3
(PRIOR ART)

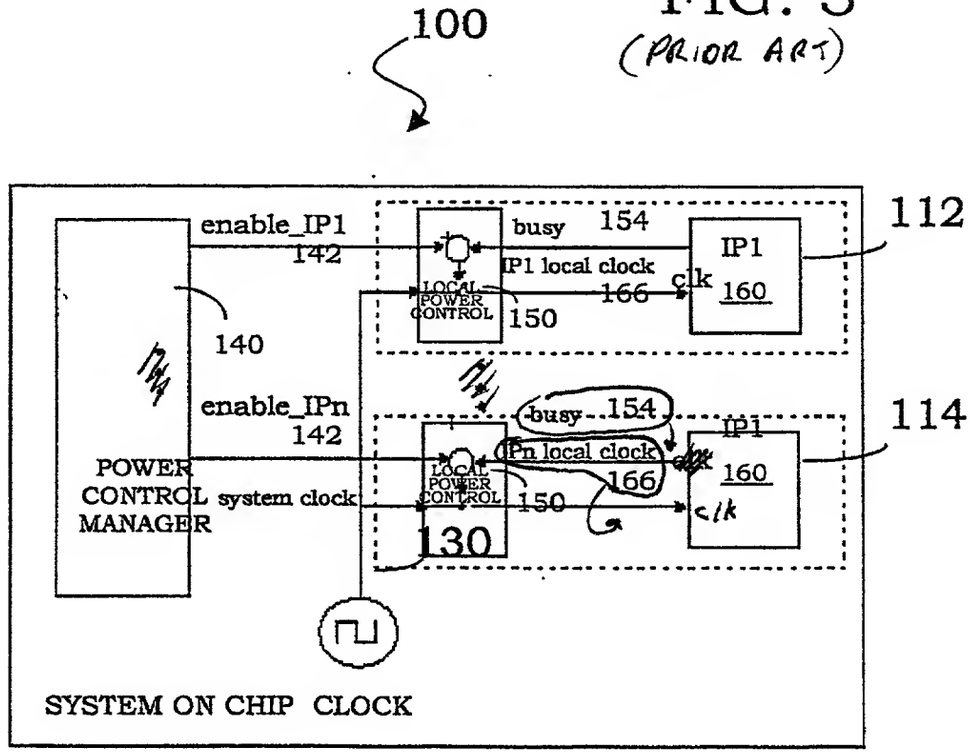

FIG. 4

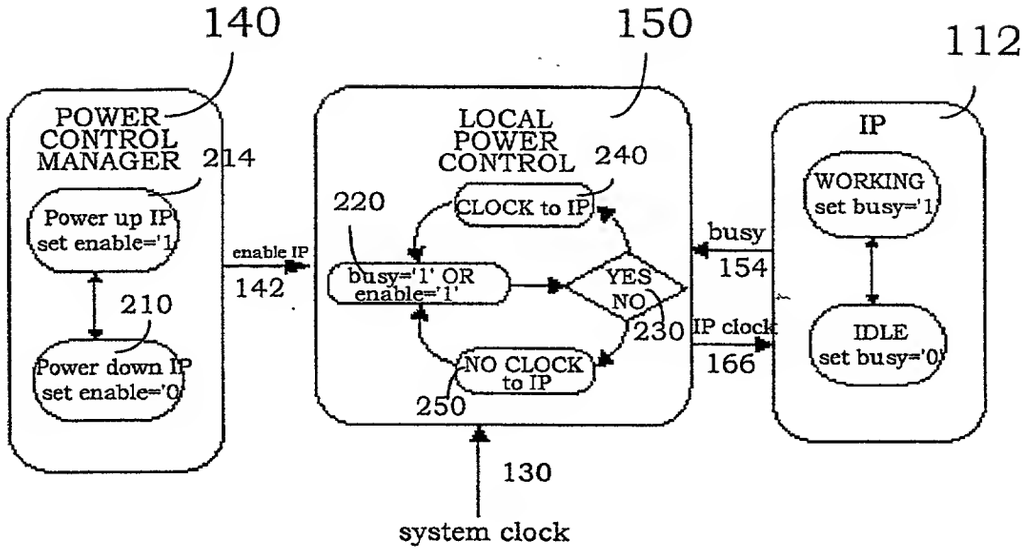

FIG. 5

```
Entering power down:

Power Down Manager:
for each IP of System
        If 'power up' IP
                set IP enable to '1';
        else
                set IP enable to '0';
        end for each;
IP:
        If 'idle' then:
                set busy to '0';
        else:
                set busy to '1';
        end if;

Local Power Control:
        If "IP busy='1' or IP enable='1'" then:
                deliver clock to IP;
        else:
                stop clock to IP
        end if;
```

190

FIG. 6

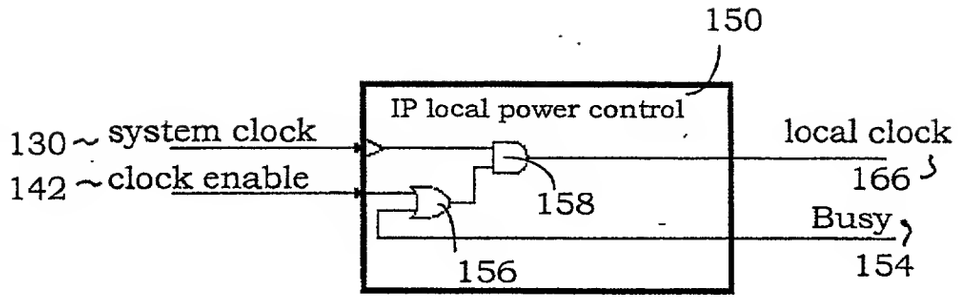
150
IP local power control
130 ~ system clock
142 ~ clock enable
158
156
local clock
166
Busy
154

FIG. 7

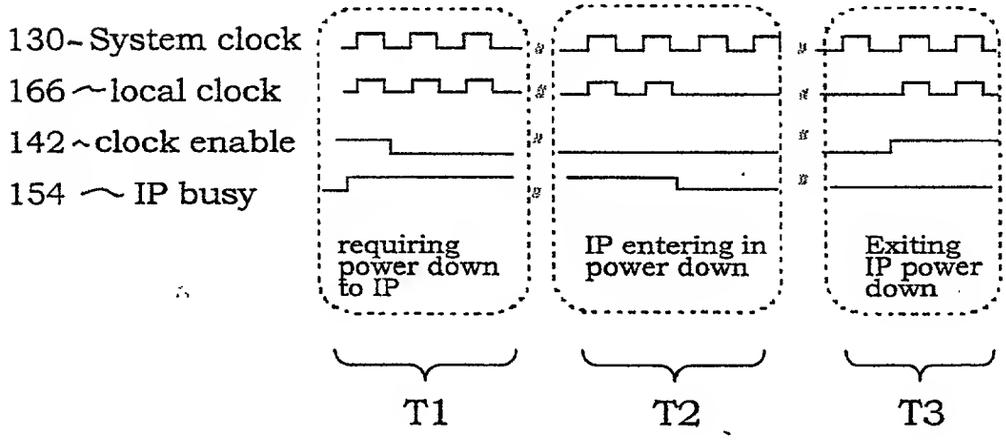
130~System clock
166 ~local clock
142 ~clock enable
154 ~ IP busy
requiring power down to IP
IP entering in power down
Exiting IP power down
T1
T2
T3

FIG. 8

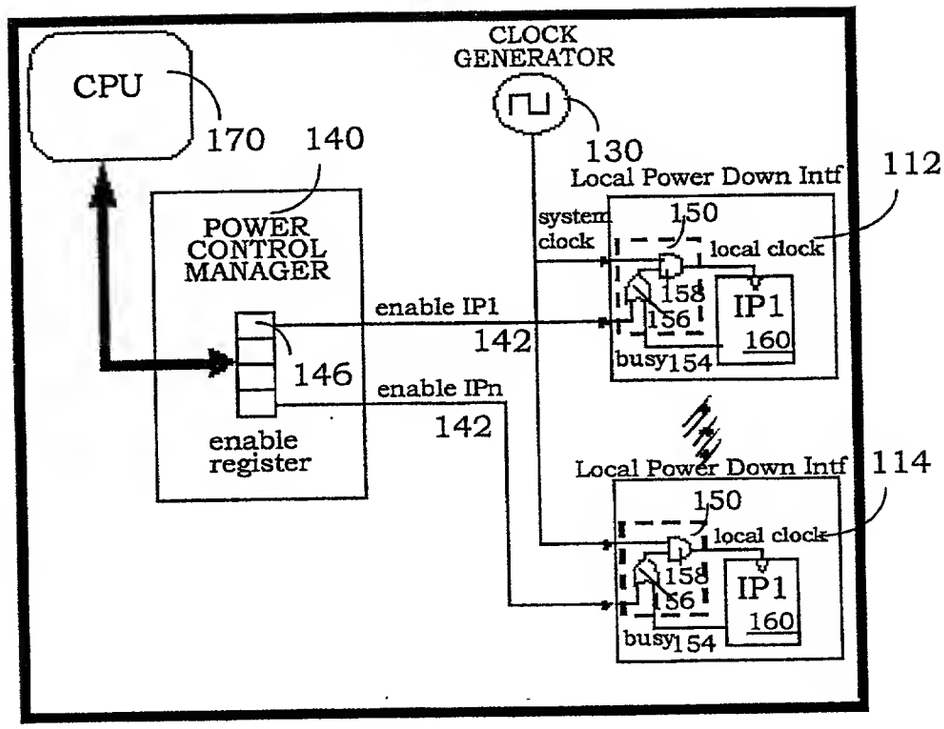
CLOCK
GENERATOR
CPU
170
140
130
Local Power Down Intf
112
POWER
CONTROL
MANAGER
system
clock
150
local clock
158
156
IP1
160
busy
154
enable IP1
142
146
enable IPn
142
enable
register
Local Power Down Intf
114
150
local clock
158
156
IP1
160
busy
154

FIG. 9